

MULTI CYCLE PIPELINED RISCv BASED PROCESSOR

TEAM 8

**Multi Cycle Pipelined RISCv Based Processor Plan**

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# CHAPTER 1 – MICRO ARCHITECTURE

## 1.1 MULTI CYCLE PIPELINED RISCv BASED PROCESSOR

A multi-cycle pipelined RISC-V based processor is a processor that leverages both multi-cycle execution and pipelining to enhance performance. Based on the RISC-V architecture, known for its simplicity and modularity, this processor divides the execution of each instruction into multiple clock cycles, while also using a pipeline to overlap the execution of multiple instructions. This combination improves throughput by processing several instructions simultaneously at different stages, balancing hardware complexity and efficiency. However, it also requires complex control logic to manage hazards and optimize pipeline performance. These processors are well-suited for applications like embedded systems, IoT devices, and general-purpose computing, where a balance of performance and cost is essential.

## 1.2 OBJECTIVES

Develop a multi-cycle 5 stage pipelined processor

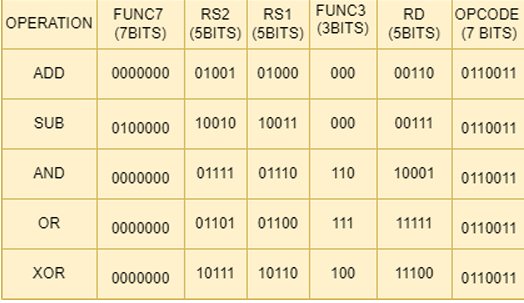
Implement and verify the functionality of below ALU operations

* ADD
* SUB
* AND
* OR
* XOR
* NOP

For each operation implement the corresponding instruction of RISCv

Also write the testbench to verify the working of the processor

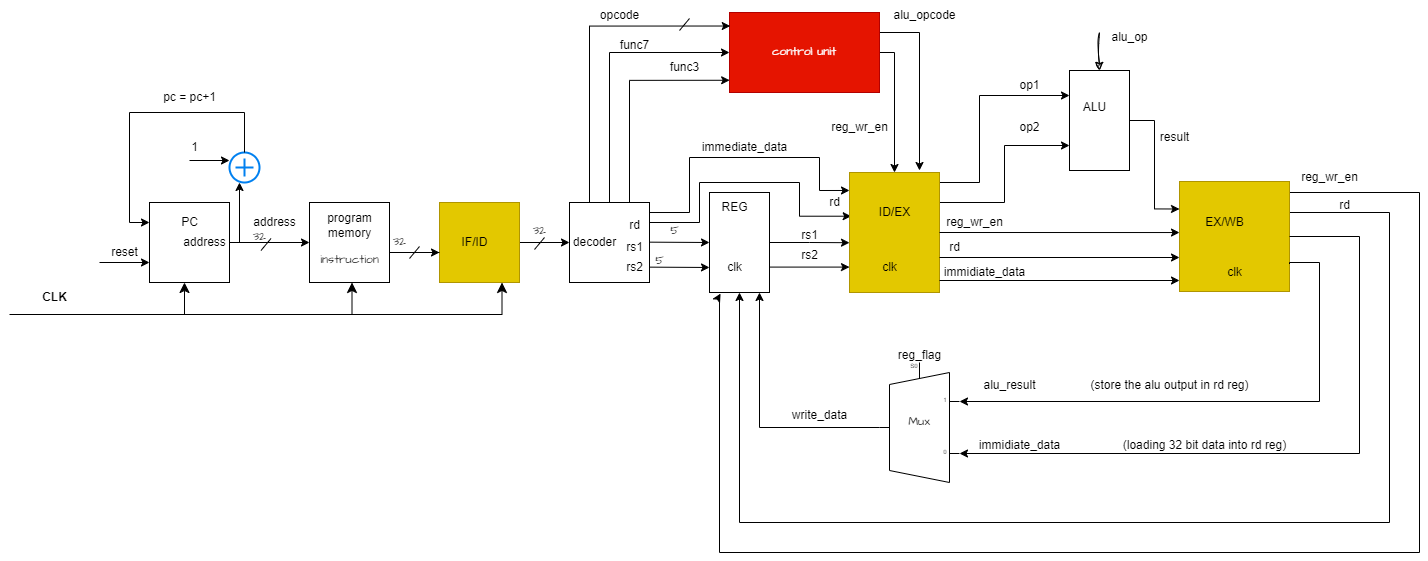
## 1.3 INSTRUCTIONS FORMAT



## 1.4 PROJECT OVERVIEW

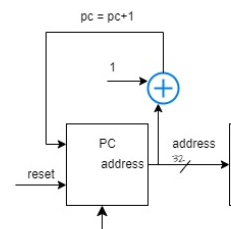
* Establishing the project's functional components and microarchitecture is designing micro-architecture.
* By utilizing the appropriate RISC-V instructions, carry out the ADD, SUB, AND, OR, XOR, and NOP algorithms.
* To confirm the processor's and each ALU operation's functionality, build a test bench.
* Construct a five-stage, multi-cycle pipelined processor design.
* Phases of a pipeline Five steps make up the processor pipeline: Write Back (WB), Memory Access (MEM), Execute (EX), Instruction Fetch (IF), and Instruction Decode (ID).
* creating multiplexers, ALUs, program counters, program memory, instruction decoders, and multiplexers, then using Verilog to create the HDL codes for those stages.

## 1.5 Micro Architecture



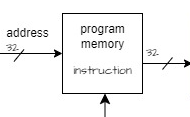
## 1.6 ARCHITECTURE COMPONENTS

### 1.6.1 Program counter:



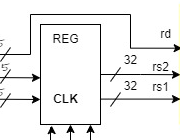
* The PC, or program counter, is a key CPU register that keeps track of the order in which instructions are executed.
* The PC is in sync with the system clock and stores the memory address of the subsequent instruction that needs to be retrieved.
* Every time there is a clock pulse, the CPU retrieves the instruction from the PC's address and advances the PC to the subsequent instruction.
* Through this procedure, the CPU is guaranteed to carry out instructions in the proper order, facilitating seamless and effective system operation.

### 1.6.2 Program memory:



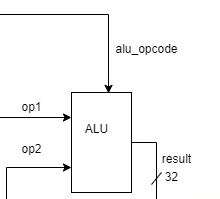
* The instructions that the CPU needs to carry out are kept in the program memory.
* The next instruction is fetched and transmitted to the control unit and decoder after the Program Counter (PC) locates its precise memory address.
* By disassembling the instruction into its constituent parts, such as register addresses, opcodes, and functions, the decoder is able to understand it. In order to guarantee that the command is carried out properly, the control unit subsequently routes this data to the relevant CPU components. Through the translation and orderly execution of instructions, this process makes it possible for the CPU to function smoothly.

### 1.6.3 Register Set:



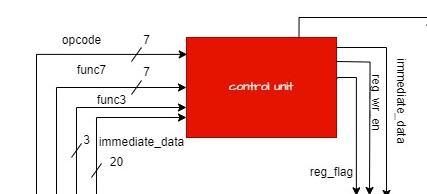
* To store the values or data needed for the ALU function or other processes, the register set consists of 16 registers with 32 bits each.

### 1.6.4 ALU:



* The Arithmetic Logic Unit (ALU) of a CPU is where all arithmetic and logic operations are carried out.
* The resultant data must be stored for later use after these processes are completed.
* Through a procedure known as "write-back," the outcome is restored into the register set.
* The CPU's registers are quick, compact storage spaces that momentarily store data.
* The CPU can swiftly retrieve the data for next operations by storing the results in registers, guaranteeing effective instruction processing and execution.

### 1.6.5 Control Unit:



* The Program Counter (PC) indicates which instruction should be fetched from memory and transmitted to the CPU's control unit.
* The instruction is interpreted and dissected into its basic parts, such as operand addresses and operation codes (opcodes), within the control unit during the decoding process.
* The CPU is then guided in correctly executing the instruction by this decoded data.